Amendments to the Claims:

Status of Claims:

Claims 1-29 are pending for examination.

Claims 1, 4, 12, 17, and 22 are in independent form.

Claims 1, 4, 12, 14, 16, 17, 22, and 26 are amended herein.

1. (Currently Amended) A method, comprising:

storing data corresponding to at least one input operating over-voltage condition occurring in an integrated circuit in an indelible memory.

2. (Original) The method of claim 1, further comprising:

determining a specified number of stored over-voltage conditions.

3. (Original) The method of claim 2, further comprising:

indicating the specified number of stored over-voltage conditions.

4. (Currently Amended) A method, comprising:

comparing an input operational condition with a specified condition:

recording data corresponding to an out-of-specification input operating condition in an indelible memory; and

determining a specified number of recorded out-of-specification input operating conditions.

5. (Previously Presented) The method of claim 4, further comprising:

detecting the out-of-specification input operating condition as an input operating over-voltage condition.

6. (Previously Presented) The method of claim 4, further comprising:

refraining from detecting the out-of-specification input operating condition for a specified amount of time.

7. (Original) The method of claim 6, wherein the specified amount of time is associated with a power-on reset time.

8. (Previously Presented) The method of claim 4, wherein the specified condition comprises a recommended operational input voltage upper limit associated with an integrated circuit.

9. (Previously Presented) The method of claim 4, wherein recording the out-of-specification input operating condition further comprises:

recording a clock speed.

10. (Previously Presented) The method of claim 9, wherein the indelible memory comprises at least one fuse.

11. (Previously Presented) The method of claim 4, wherein determining the specified number of recorded out-of-specification input operating conditions further comprises:

reading a signature value stored in the indelible memory.

12. (Currently Amended) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

comparing an input operational voltage with a specified voltage;

recording a value corresponding to an input operating over-voltage condition in an indelible memory; and

determining a specified number of recorded input operating over-voltage conditions.

13. (Previously Presented) The article of claim 12, wherein the data, when accessed, results in the machine performing:

filtering the input operational voltage for at least a duration of one clock period.

14. (Currently Amended) The article of claim 12, wherein recording the value corresponding to the input operating over-voltage condition further comprises:

recording the value corresponding to the input operating over-voltage condition only if the input operational voltage is greater than the specified voltage by a selected amount.

15. (Original) The article of claim 14, wherein the selected amount is at least about two times greater than an expected noise voltage value.

16. (Currently Amended) The article of claim 12, wherein the data, when accessed, results in the machine performing:

verifying recordation of the value corresponding to the input operating over-voltage condition.

17. (Currently Amended) An apparatus, comprising:

an indelible memory to store information corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit.

18. (Previously Presented) The apparatus of claim 17, further comprising:

a detection module coupled to the indelible memory to determine the existence of at least one of the selected number of out-of-specification input operational conditions.

19. (Previously Presented) The apparatus of claim 18, further comprising:

a filter module coupled to the detection module.

20. (Original) The apparatus of claim 17, wherein the indelible memory comprises a fuse.

21. (Previously Presented) The apparatus of claim 17, wherein at least one of the out-of-specification input operational conditions comprises an over-voltage condition.

22. (Currently Amended) A system, comprising:

an indelible memory to store data corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit; and

a display coupled to the electronic circuit.

23. (Original) The system of claim 22, wherein the electronic circuit comprises a microprocessor.

24. (Previously Presented) The system of claim 22, further comprising:

a logic module to detect each one of the selected number of out-of-specification input operational conditions.

25. (Original) The system of claim 24, wherein the logic module comprises an analog-to-digital converter.

26. (Currently Amended) The system of claim 22, further comprising:

a second memory to store data corresponding to a specified condition to be compared with an operational condition associated with the electronic circuit.

27. (Previously Presented) The system of claim 26, wherein the specified condition comprises a recommended operational input voltage upper limit associated with an integrated circuit.

28. (Original) The system of claim 27, wherein the integrated circuit comprises a microprocessor.

29. (Previously Presented) The system of claim 22, further comprising:

a basic input-output system to determine the selected number of out-of-specification input operational conditions.